

Application Serial No. 09/434,394

Attorney Docket No. 114596-20 4009

Amendment Dated October 11, 2006 - Request for Reconsideration of Action of July 18, 2006

**CLAIMS**

1           1. (previously presented) A computer, comprising:  
2           a binary translator programmed to translate at least a segment of a binary representation  
3 of a program from a first representation in a first instruction set architecture to a second  
4 representation in a second instruction set architecture, a sequence of side-effects in the second  
5 representation differing from a sequence of side-effects in the translated segment of the first  
6 representation, the second representation distinguishing individual memory loads that are  
7 believed to be directed to well-behaved memory from memory loads that are believed to be  
8 directed to non-well-behaved memory device(s);  
9           instruction execution circuitry designed, while executing the second representation,  
10           to identify an individual memory-reference instruction, or an individual memory  
11 reference of an instruction, a side-effect arising from the memory reference having been  
12 reordered by the translator, the memory reference having been believed at translation time to be  
13 directed to well-behaved memory but that at execution time is found to reference a device with a  
14 valid memory address that cannot be guaranteed to be well-behaved, based at least in part on an  
15 annotation encoded in a segment descriptor, and  
16           based in the distinguishing, to identify whether the difference in sequence of side-  
17 effects may have a material effect on the execution of the program; and  
18           circuitry and/or software designed to establish program state to a state equivalent to a  
19 state that would have occurred in the execution of the first representation, and to resume  
20 execution of the translated segment of the program in the first instruction set.

Amendment After Final  
This paper dated October 11, 2006

page  
2

114596-20-4009 S/N 09/434,394  
3360903.3

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Application Serial No. 09/434,394  
Attorney Docket No. 114596-20-4009  
Amendment Dated October 11, 2006 - Request for Reconsideration of Action of July 18, 2006

1           2. (currently amended) A method, comprising the step of:  
2           for memory references generated as part of executing a stream of instructions on a  
3 computer, evaluating whether an individual memory reference of an instruction references a  
4 device having a valid memory address but that cannot be guaranteed to be well-behaved, based at  
5 least in part on an annotation encoded in a segment descriptor, a segment descriptor being data  
6 for controlling physical address formation by designating a segment base address, a segment  
7 length, and segment access control information.

          3. (original) A method of claim 2, further comprising the step of:  
          if the reference cannot be guaranteed to be well-behaved, re-executing the instruction in  
an alternative execution mode.

          4. (previously presented) The method of claim 3, further comprising the step of:  
          while translating at least a segment of a binary representation of a program from a first  
instruction set architecture to a second instruction set architecture to produce the stream of  
instructions, annotating in the produced instructions memory loads that are believed to be  
directed to well-behaved memory from memory loads that are believed to be directed to non-  
well-behaved memory.

          5. (original) A method of claim 2, further comprising the step of:  
          for memory references generated as part of executing a stream of instructions on a  
computer, evaluating whether an individual memory reference of an instruction has been  
reordered relative to other side-effects in a manner that materially alters the execution of a  
program of the memory reference.

          6. (previously presented) The method of claim 2, further comprising the step of:  
          if the reference cannot be guaranteed to be well-behaved, rolling back the state of the  
instruction stream to a prior state.

Amendment After Final  
This paper dated October 11, 2006

page  
3

114596-20-4009

S/N 09/434,394  
3360903.3

Application Serial No. 09/434,394

Attorney Docket No. 114596-20-4009

Amendment Dated October 11, 2006 – Request for Reconsideration of Action of July 18, 2006

7. (previously presented) The method of claim 6, wherein  
the rolling back step is initiated when an exception occurs in an object program generated  
by binary translation from a reference implementation source program.

8. (original) A method of claim 6, further comprising the step of:  
resuming executing from the rolled back state, the resumed execution executing a precise  
side-effect emulation of the reference implementation.

9. (original) A method of claim 2, wherein the device having a valid memory address  
has an address in an I/O space of the computer.

10. (previously presented) The method of claim 2, further comprising evaluating an  
annotation embedded in the instruction to determine whether the reference to the device that  
cannot be guaranteed to be well-behaved is to raise an exception.

11. (previously presented) The method of claim 2, further comprising the step of:  
in circuitry embedded in address translation circuitry of the computer, evaluating whether  
the reference to the device that cannot be guaranteed to be well-behaved is to raise an exception.

12. (previously presented) The method of claim 2, wherein the segment descriptor is  
stored in a segment register.

13. (original) A method of claim 2, further comprising forming the segment descriptor  
by copying another segment descriptor, and altering the annotation.

Amendment After Final  
This paper dated October 11, 2006

page  
4

114596-20-4009

S/N 09/434,394  
3360903.3

Application Serial No. 09/434,394

Attorney Docket No. 114596-20-4009

Amendment Dated October 11, 2006 - Request for Reconsideration of Action of July 18, 2006

1           14. (currently amended) A computer, comprising:  
2           instruction execution circuitry designed to evaluate, based at least in part on an  
3           annotation encoded in a segment descriptor, a segment descriptor being data for controlling  
4           physical address formation by designating a segment base address, a segment length, and  
5           segment access control information, whether an individual memory-reference instruction, or an  
6           individual memory reference of an instruction, references a device with a valid memory address  
7           that cannot be guaranteed to be well-behaved.

15. (original) A computer of claim 14, further comprising:  
binary translator software programmed to generate the memory-reference instruction.

16. (original) A computer of claim 15, wherein the binary translator is further  
programmed to annotate the memory-reference instruction with an indication of whether the  
memory-reference instruction is likely or unlikely to reference well-behaved memory.

17. (previously presented) The computer of claim 14, further comprising:  
a translator programmed to translate at least a segment of a source program into an object  
program, wherein a sequence of side-effects in the object program differs from a reference  
sequence of side-effects in the source program; and  
circuitry and/or software designed to intervene during an execution of the object program  
on the computer to establish a program state equivalent to a state that would have occurred in the  
reference sequence, and to resume execution of the program from the established state in an  
execution mode that reflects the reference side-effect sequence.

18. (original) A computer of claim 14, wherein:  
code in a preamble of a program unit embracing the memory-reference instruction  
establishes a state of the instruction execution circuitry, the instruction execution circuitry

Amendment After Final  
This paper dated October 11, 2006

page  
5

114596-20-4009

S/N 09/434,394  
3360903.3

Application Serial No. 09/434,394  
Attorney Docket No. 114596-20-4009  
Amendment Dated October 11, 2006 - Request for Reconsideration of Action of July 18, 2006

designed to raise an exception based on an evaluation of both the state and the evaluation of the reference to the device.

19. (original) A computer of claim 14, further comprising circuitry to raise an exception based on an evaluation of both an annotation embedded in the instruction and the evaluation of the reference to the device.

20. (original) A computer of claim 14, further comprising circuitry in an address translation path to raise an exception of a computer based on the evaluation of the reference to the device.

21. (original) A computer of claim 14, further comprising circuitry to raise an exception based on an evaluation of both a segment descriptor and the evaluation of the reference to the device.

1        22. (currently amended) A method, comprising the steps of:  
2        while translating at least a segment of a binary representation of a program from a first  
3        instruction set architecture to a second representation in a second instruction set architecture,  
4        distinguishing individual memory loads that are believed to be directed to well-behaved memory  
5        from memory loads that are believed to be directed to non-well-behaved memory device(s);  
6        while executing the second representation, identifying a load that was believed at  
7        translation time to be directed to well-behaved memory but that at execution time is found to be  
8        directed to non-well-behaved memory, based at least in part on an annotation encoded in a  
9        segment descriptor, and aborting the identified memory load, a segment descriptor being data for  
10       controlling physical address formation by designating a segment base address, a segment length,  
11       and segment access control information; and  
12       based at least in part on the identifying, re-executing at least a portion of the translated  
13       segment of the program in the first instruction set.

Amendment After Final  
This paper dated October 11, 2006

page  
6

114596-20-4009

S/N 09/434,394  
3360903.3

Application Serial No. 09/434,394  
Attorney Docket No. 114596-20-4009  
Amendment Dated October 11, 2006 - Request for Reconsideration of Action of July 18, 2006

23. (original) A method of claim 22, further comprising the steps of:  
while executing the translation, detecting an ordering of side-effects that differs from the reference sequence of side-effects of the binary representation in the first instruction set architecture;  
establishing the state of the translated program to a state equivalent to a state that would have occurred in the binary representation in the first instruction set architecture; and  
resuming execution of the program from the established state in an execution mode that reflects the reference side-effect sequence.

24. (original) A method of claim 23, wherein the difference of ordering of side-effects includes a reordering of two side-effects relative to each other.

25. (original) A method of claim 23, wherein the difference of ordering of side-effects includes an elimination of a side-effect by the translating.

26. (previously presented) The method of claim 22, further comprising the step of:  
annotating the second representation with an indication of the distinction between individual memory loads that are believed to be directed to well-behaved memory from memory loads that are believed to be directed to non-well-behaved memory.

27. (previously presented) The method of claim 22, further comprising the step of:  
executing code in a preamble of the second representation to establish a state of instruction execution circuitry, the instruction execution circuitry designed to raise an exception based on an evaluation of both the state and the identification of loads.

Amendment After Final  
This paper dated October 11, 2006

page  
7

114596-20-4009

S/N 09/434,394  
3360903.3

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Application Serial No. 09/434,394  
Attorney Docket No. 114596-20-4009  
Amendment Dated October 11, 2006 - Request for Reconsideration of Action of July 18, 2006

28. (previously presented) The method of claim 22, further comprising evaluating an annotation embedded in the instruction of the identified load to determine whether to raise an exception.

29. (previously presented) The method of claim 22, further comprising the step of:  
in circuitry embedded in address translation circuitry, evaluating whether the instruction of the identified load is to raise an exception.

1 30. (currently amended) An apparatus, comprising:  
2 a binary translator programmed to translate at least a segment of a binary representation  
3 of a program from a first instruction set architecture to a second representation in a second  
4 instruction set architecture, distinguishing individual memory loads that are believed to be  
5 directed to well-behaved memory from memory loads that are believed to be directed to non-  
6 well-behaved memory; and  
7 instruction execution circuitry designed to execute the translated program in the second  
8 representation, and to identify, based at least in part on an annotation encoded in a segment  
9 descriptor, a segment descriptor being data for controlling physical address formation by  
10 designating a segment base address, a segment length, and segment access control information,  
11 memory loads that were believed at translation time to be directed to well-behaved memory but  
12 that at execution time are found to be directed to non-well-behaved memory, and to abort the  
13 identified memory load.

31. (original) A apparatus of claim 30, further comprising:  
hardware designed to re-execute at least a portion of the translated segment of the  
program in the first instruction set.

Amendment After Final  
This paper dated October 11, 2006

page  
8

114596-20-4009

S/N 09/434,394  
3360903.3

Application Serial No. 09/434,394

Attorney Docket No. 114596-20-4009

Amendment Dated October 11, 2006 - Request for Reconsideration of Action of July 18, 2006

32. (previously presented) The apparatus of claim 30, wherein:

the binary translator is further programmed to produce a sequence of side-effects in the second representation differing from a sequence of side-effects in the translated segment of the first representation; and

the instruction execution circuitry is further designed to identify cases during execution of the second representation in which the difference in sequence of side-effects may have a material effect on the execution of the program, to establish program state to a state equivalent to a state that would have occurred in the execution of the first representation, and to resume execution of the program from the established state in an execution mode that reflects the side-effect sequence of the first representation.

33. (previously presented) The apparatus of claim 32, wherein the difference of sequence of side-effects includes a reordering of two side-effects relative to each other.

34. (previously presented) The apparatus of claim 32, wherein the difference of sequence of side-effects includes an elimination of a side-effect by the translating.

35. (previously presented) The apparatus of claim 30, further comprising the step of: annotating the second representation with an indication of the distinction between individual memory loads that are believed to be directed to well-behaved memory from memory loads that are believed to be directed to non-well-behaved memory.

36. (original) A apparatus of claim 30, wherein the device having a valid memory address has an address in an I/O space of a computer.

37. (previously presented) The apparatus of claim 30, further comprising evaluating an annotation embedded in the instruction of the identified load to determine whether to raise an exception.

Amendment After Final  
This paper dated October 11, 2006

page  
9

114596-20-4009

S/N 09/434,394  
3360903.3



Application Serial No. 09/434,394

Attorney Docket No. 114596-20-4009

Amendment Dated October 11, 2006 - Request for Reconsideration of Action of July 18, 2006

38. (previously presented) The apparatus of claim 30, further comprising:  
in circuitry embedded in address translation circuitry for the instruction execution  
circuitry, evaluating whether the instruction of the identified load is to raise an exception.

39. (previously presented) The apparatus of claim 30, further comprising circuitry to  
raise an exception based on an evaluation of both a segment descriptor and the evaluation of the  
reference to non-well-behaved memory.

1        40. (previously presented) A method, comprising the steps of:  
2        translating at least a segment of a source program into an object program, the source  
3        program instructing a reference execution with a reference sequence of side-effects, the object  
4        program instructing an execution in which the sequence of side-effects differs from the reference  
5        sequence;  
6        during an execution of the object program on a computer, detecting a side-effect about to  
7        be committed to processor state in which the differing side-effect sequence may have a material  
8        effect on the execution of the program, and aborting the side-effect;  
9        establishing a program state equivalent to a state that would have occurred in the  
10       reference execution; and  
11       resuming execution of the program from the established state in an execution mode that  
12       reflects the reference side-effect sequence.

41. (original) A method of claim 40, wherein the source program is coded in a first  
instruction set architecture, and the object program is coded in a second instruction set  
architecture.

Amendment After Final  
This paper dated October 11, 2006

page  
10

114596-20-4009

S/N 09/434,394  
3360903.3

Application Serial No. 09/434,394  
Attorney Docket No. 114596-20-4009  
Amendment Dated October 11, 2006 - Request for Reconsideration of Action of July 18, 2006

42. (previously presented) The method of claim 41, further comprising the steps of:  
evaluating, based at least in part on an annotation encoded in a segment descriptor,  
whether an individual memory reference of an instruction initiated by execution the object  
program references a device having a valid memory address but that cannot be guaranteed to be  
well-behaved; and

initiating the establishing step based at least in part on the evaluating.

43. (previously presented) The method of claim 41, further comprising the step of:  
annotating the object program with an indication of a distinction between individual  
memory references that are believed to be directed to well-behaved memory from memory  
references that are believed to be directed to non-well-behaved memory.

44. (previously presented) The method of claim 41, further comprising the step of:  
executing code in a preamble of the object program to establish a state of instruction  
execution circuitry, the instruction execution circuitry designed to raise an exception based on an  
evaluation of both the state and the evaluation of individual memory references.

45. (previously presented) The method of claim 41, further comprising evaluating an  
annotation embedded in the instruction of the individual side-effect to determine whether to raise  
an exception.

46. (previously presented) The method of claim 41, further comprising the step of:  
in circuitry embedded in address translation circuitry of the computer, evaluating whether  
the instruction of the individual side-effect is to raise an exception.

47. (original) A method of claim 41, further comprising the step of:  
raising an exception based on an evaluation of both a segment descriptor and the  
evaluation of the side-effect.

Amendment After Final  
This paper dated October 11, 2006

page  
11

114596-20-4009

S/N 09/434,394  
3360903.3

Application Serial No. 09/434,394  
Attorney Docket No. 114596-20-4009  
Amendment Dated October 11, 2006 - Request for Reconsideration of Action of July 18, 2006

48. (original) A method of claim 41, further comprising:  
evaluating an annotation encoded in a segment descriptor to determine whether the  
reference to the non-well-behaved device is to raise an exception.

49. (original) A method of claim 41, further comprising forming the segment descriptor  
by copying another segment descriptor, and altering the annotation.

50. (original) A method of claim 41, further comprising copying into the formed  
segment descriptor a variable indicating an assumed sensitivity of the translation to alteration of  
the sequence of side-effects.

51. (original) A method of claim 41, wherein the difference of ordering of side-effects  
includes a reordering of two side-effects relative to each other.

52. (original) A method of claim 41, wherein:  
the establishing step is initiated when an exception occurs in the object program.

53. (previously presented) The method of claim 41, further comprising the step of:  
resuming execution from the established state, the resumed execution executing a precise  
side-effect emulation of the reference execution.

54. (original) A method of claim 41, further comprising the step of:  
using a descriptor generated during the translation to establish a pre-exception reference  
state.

Amendment After Final  
This paper dated October 11, 2006

page  
12

114596-20-4009

S/N 09/434,394  
3360903.3

Application Serial No. 09/434,394  
Attorney Docket No. 114596-20-4009  
Amendment Dated October 11, 2006 - Request for Reconsideration of Action of July 18, 2006

1           55. (previously presented) An apparatus, comprising:  
2           a binary translator programmed to translate at least segment of a program from a first  
3 representation in a first instruction set architecture to a second representation in a second  
4 instruction set architecture, a sequence of side-effects in the second representation differing from  
5 a sequence of side-effects in the translated segment of the first representation; and  
6           instruction execution circuitry and/or software designed to  
7           identify cases during execution of the second representation in which the  
8 difference in sequence of side-effects may have a material effect on the execution of the  
9 program, before committing the side-effect to processor state, and aborting the side-effect; and  
10           to establish a program state equivalent to a state that would have occurred in the  
11 execution of the first representation, and to resume execution of the program from the  
12 established state in an execution mode that reflects the side-effect sequence of the first  
13 representation.

56. (original) A apparatus of claim 55, further comprising:  
annotating the second representation with an indication of the distinction between  
individual memory loads that are believed to be directed to well-behaved memory from memory  
loads that are believed to be directed to non-well-behaved memory.

57. (previously presented) The apparatus of claim 56, wherein:  
the instruction execution circuitry is designed to evaluate an annotation embedded in the  
instruction of the identified load to determine whether to raise an exception.

58. (previously presented) The apparatus of claim 56, further comprising:  
in circuitry embedded in address translation circuitry for the instruction execution  
circuitry, evaluating whether the instruction of the identified load is to raise an exception.

Amendment After Final  
This paper dated October 11, 2006

page  
13

114596-20-4009

S/N 09/434,394  
3360903.3

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Application Serial No. 09/434,394  
Attorney Docket No. 114596-20-4009  
Amendment Dated October 11, 2006 - Request for Reconsideration of Action of July 18, 2006

59. (previously presented) The apparatus of claim 56, further comprising:  
circuitry to evaluate an annotation encoded in a segment descriptor to determine whether  
a reference to a device in non-well-behaved memory is to raise an exception.

60. (cancelled)

61. (previously presented) The apparatus of claim 55, wherein the difference of  
sequence of side-effects includes a reordering of two side-effects relative to each other.

62. (previously presented) The apparatus of claim 55, wherein the difference of  
sequence of side-effects includes an elimination of a side-effect .

63. (previously presented) The apparatus of claim 55, wherein the difference of  
sequence of side effects results from combining two side-effects in the binary translator.

64. (previously presented) The apparatus of claim 55, wherein:  
the establishing is initiated when an exception occurs in the second representation.

65. (previously presented) The apparatus of claim 55, wherein:  
the resumed execution executes a precise side-effect emulation of the first representation.

Amendment After Final  
This paper dated October 11, 2006

page  
14

114596-20-4009

S/N 09/434,394  
3360903.3